IN THE CLAIMS

Please amend the claims as follows:

1 -19. (Canceled)

20. (Currently Amended) ~~The~~ A processor ~~of claim 13,~~ comprising:

an instruction pipeline, wherein the pipeline is two instructions wide;

a results pipeline, wherein the instruction pipeline and the results pipeline are counter rotating queues;

a first execution unit in communication with the results and instruction pipelines;

a plurality of threads including a first and second thread;

a first and a second reorder buffer, the first reorder buffer associated with the first thread and the second reorder buffer associated with the second thread; and

a first instruction fetch/decode unit.

21. (New) The processor of claim 20, wherein instructions from the first instruction fetch/decode unit are multiplexed into the first and second threads and into points spaced evenly at first and second locations around the instruction and results pipelines.

22. (New) The processor of claim 21, further including a second execution unit, wherein the first and second execution unit are spaced evenly around the instruction and results pipeline.